

## **REMARKS**

Applicant would like to thank the Examiner for the careful consideration given the present application. The application has been carefully reviewed in light of the Office action, and amended as necessary to more clearly and particularly describe the subject matter which applicant regards as the invention.

The Examiner rejected claims 1-3 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant notes that claim 1 has been amended and, thus, respectfully requests removal of the rejection.

The Examiner rejected claims 1 and 2 under 35 U.S.C. 103(a) as being unpatentable over Okura et al., U.S. Pat. Pub. No. 2003/0052400 in view of Applicant's admitted prior art (hereinafter "AAPA"). The Examiner's rejection is traversed for the following reason.

In regards to claim 1, Applicant has amended claim 1 to further differentiate the present invention over the cited prior art. Specifically, Applicant has amended claim 1 to clarify that a gap exists between the passivation layer and the upper heat-sinking part, which Applicant respectfully contends is not taught by the cited prior art.

Accordingly, Applicant discloses a semiconductor device module structure that includes a ring guard part. The ring guard part includes a passivation layer, which covers the insulating layer without covering the cell region. Further, a gap is formed between the passivation layer and the upper heat-sinking part. Thus, the passivation layer does not directly contact the upper heat-sinking part.

Applicant would like to emphasize that the gap formed between the

passivation layer and the upper heat-sinking part is an empty space. Specifically, there is no solder or the like present in the gap or empty space. The gap or empty space allows for thermal expansion of both the upper heat-sinking part and the passivation film, which in turn eliminates thermal stresses between layers in the semiconductor element. As an advantageous result, cracks are prevented in a silicon board, which in turn prevents a voltage withstandability drop caused by the cracks in the silicon board.

Okura, on the other hand, discloses a semiconductor device that has a heat sink soldered to one surface of the semiconductor element and a heat sink soldered to the opposite surface of the semiconductor element. Okura, however, does not disclose a gap between the heat sink and any other component on the semiconductor device.

Accordingly, Okura does not teach all the features, for which it is cited, of claim 1. More specifically, Okura does not teach "wherein a gap is formed between the passivation layer and the upper heat-sinking part such that the passivation layer does not directly contact the upper heat-sinking part."

Rather, referring to paragraph [0049] and to FIGS. 1 and 8 of Okura, Okura discloses a gate wiring layer 2 formed on the surface of the semiconductor element 1 and a protective (passivation) film 3 formed to cover the wiring layer 2. A heat sink block 4 is bonded to the protective film 3 with solder 5. FIG. 1 clearly shows that the heat sink 4 is in contact, via the solder 5, with the protective film 3. Thus, a gap does not exist between the heat sink 4 and the protective film 3 (passivation layer), as required by claim 1 of the present invention. Therefore, Okura does not teach a gap between the passivation layer and an upper heat-sinking part.

Based on the foregoing, it is apparent that Okura does not teach all the features of claim 1, for which it is cited. Thus, reconsideration and withdrawal of the rejections of claim 1 based upon Okura are hereby requested.

Further, in regards to AAPA, Applicant submits that AAPA does not correct or eliminate the deficiencies of the primary reference, Okura. Referring to FIGS. 5 and 6 in AAPA, AAPA does not teach an upper heat sink. Thus, AAPA does not correct or eliminate the deficiencies of Okura. Therefore, Applicant submits that claim 1 is allowable over the proposed combination of the references.

Claim 2 depends from claim 1, thus, all arguments pertaining to claim 1 are equally applicable to claim 2 and are herein incorporated by reference.

The Examiner rejected claim 3 under 35 U.S.C. 103(a) as being unpatentable over Okura et al., U.S. Pat. Pub. No. 2003/0052400 and Applicant's admitted prior art (hereinafter "AAPA"), as applied to claim 1 above, further in view of Hirano et al., U.S. Pat. Pub. No. 2003/0122232. The Examiner's rejection is traversed for the following reason.

Claim 3 depends from claim 1, thus, all arguments pertaining to claim 1 are equally applicable to claim 3 and are herein incorporated by reference.

Further, Applicant submits that Hirano does not correct or eliminate the deficiencies of the primary reference, Okura, as they relate to claim 1. Hirano discloses a semiconductor power device that includes a semiconductor element 11, a lower heat sink 13, and an upper heat sink 14. Hirano, however, does not disclose or suggest that a gap exists between the upper heat sink 14 and the protective film in the semiconductor element 1. Thus, Hirano does not correct or eliminate the deficiencies of Okura, as they relate to claim 1. Therefore, Applicant submits that

claim 3 is allowable over the proposed combination of the references.

In regards to new claim 4, claim 4 depends from claim 1, thus, all arguments pertaining to claim 1 are equally applicable to claim 4 and are herein incorporated by reference.

In light of the foregoing, it is respectfully submitted that the present application is in a condition for allowance and notice to that effect is hereby requested. If it is determined that the application is not in a condition for allowance, the Examiner is invited to initiate a telephone interview with the undersigned attorney to expedite prosecution of the present application.

If there are any additional fees resulting from this communication, please charge same to our Deposit Account No. 18-0160, our Order No. SHM-16693.

Respectfully submitted,

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